# IN-DEPTH SIMULATION ANALYSIS OF THE SI-SIO2 INTERFACE TRAPS BY THE CHARGE PUMPING

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## ABSTRACT

The purpose of this work is to contribute to a better electrical characterization of the Silicon-Oxide interface By the Three level charge pmping.

The introduction of a third voltage level in the gate pulse gives access to the same parameters as the two charge pumping but requires less simplifying assumptions.

We show that the three charge pumping and its variants are powerful tools to determine the $D_{it}$ (E) and $\sigma$ (E) distribution.

The simulated results are in a good agreement with recent and different experimental results

## KEYWORDS

Si-$SiO_2$ Interface, Fast States, Slow States, Defect Profile, Charge Pumping

## INTRODUCTION

The charge pumping (Cp) technique is a powerful tool used to characterize the traps of the Si-$Sio_2$ interface in submicrometer MOS devices. It has based on the exploitation of a repetitive process where by majority carriers coming from the substrate recombine with minority carriers previously trapped in interface states, when the MOSFET is submitted to well-chosen biasing cycles [1].

By adjusting some experimental parameters, we also gain access to the energy distribution of the states $D_{it}$ (E) and to their spatial distribution $D_{it}(x)$.

Given the shrinking dimensions of elementary transistors, the various charge-pumping techniques are to date the only techniques, which make it possible to characterize the Si-$Sio_2$ interface directly in the transistor it self. They thus a promising future.

Recently, Saks and Ancona have proposed a technique that is the most complete synthesis of the three-level charge pumping procedures already published [2]. One originality of our work was to apply, for the first time, this charge pumping method to submicronic MOS transistors in order to characterize, with a high sensitivity, the electron interface states. In our paper, we show that, the sensitivity of this three-level technique can be increased, this method can be applied to transistors with low interface states densities, electron capture cross sections of these devices depend on energy and a simple calculation allows to take into account this variation with energy without requiring a particular formalism and to obtain the energetic distribution on a domain including the silicon bandgap.

## THREE-LEVEL CHARGE PUMPING THEORY

In three-level Charge pumping technique, a three-level gate voltage pulse, as represented in figure 1, is applied to the transistor gate. When the semiconductor surface is inverted, the system is below the Fermi level $E_F$ are filled by substrate minority carries (electrons for a n-channel transistor), while interface states above $E_F$ are empty.

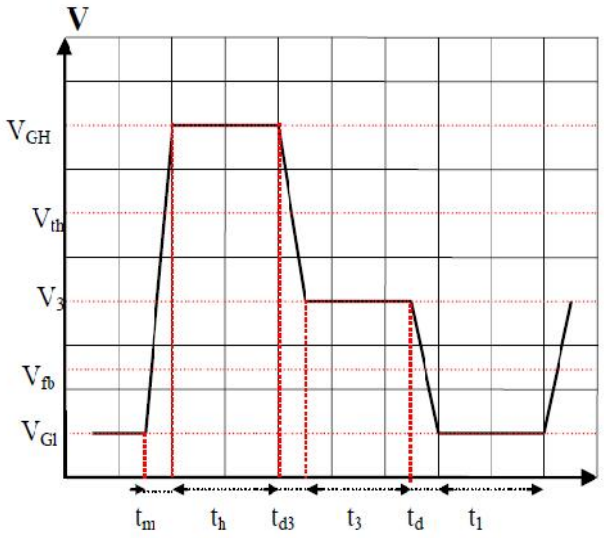


Figure.1 Gate voltage signal used in three-level charge pumping for the determination of emission times of electron interface states on N-channel MOS transistor

When the gate potential is switched to $V_3$, many electrons are emitted back to the conduction band by interface states. The occupancy factor of these states tends towards the one corresponding to thermodynamic equilibrium. But interface states above $E_F$ emit their electrons only if their electron emission time $\tau_e$ is less than to $t_3$. Switching the transistor to strong accumulation drifts holes towards the $Si/SiO_2$ interface. These holes recombine with electrons remained trapped in interface states, giving rise to the charge pumped into the substrate. For a p channel transistor, complementary gate voltage pulses are applied to the gate (obtained by changing all the signs of the biases). By varying the intermediate gate voltage parameters, i.e. bias $V_3$ and time $t_3$, one can select interface states which are involved at each charge pumping technique cycle. One of the energetic limits of the domain scanned in the silicon bandgap depends on the value of $V_3$ whereas the value of $t_3$ determines which are the traps, into this energetic window, that can emit their electrons. Only interface states having a time constant $\tau_e$ verifying $t_{rf}<\tau_e< t_3$ are detected [3]. The emission time window can be adjusted by varying $t_r$ and $t_3$. This modulation,

in bias and/or in emission time is the basic principle of all three-level charge pumping technique recently developed [4]. If $V_{31}$is changing to $V_{32}$ for a fixed $t_{31}$ (figure2), the equilibrium occupancy level of the traps will change.

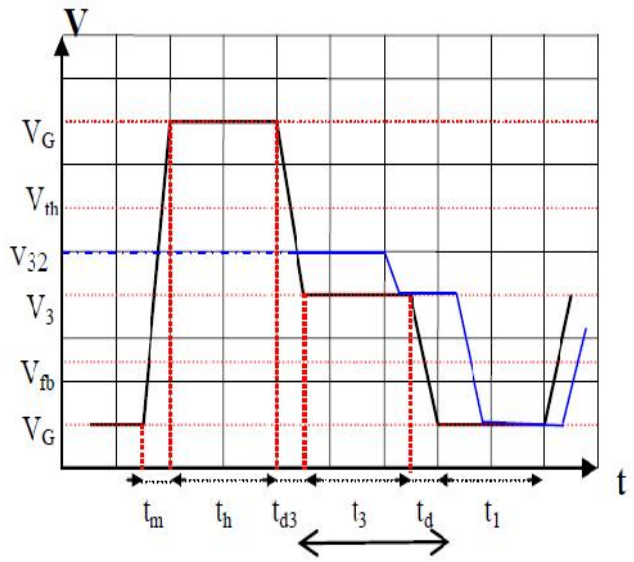


Figure.2 Variations of the parameters of the three-level gate voltage signal allowing the energy sweeping (variations of $V_3$) and the emission time sweeping (variations of $t_3$).

The electron interface states density, between $E_{F1}$ and $E_{F2}$ (respectively determined by $V_{31}$ and $V_{32}$) with a time constant $\tau_e$ verifying $trf1<\tau_e< t_{31}$ can be deduced from the corresponding variation of the charge pumped into the substrate:

$$D_{it}(E_t) = \frac{dQ_{it}dV_3}{qA_{eff}dV_3d\Psi_3} \qquad (1)$$

Where $Q_{it}$ is the charge pumped per cycle and $A_{eff}$ is the channel effective area. $Q_{it\ depends}$ on the source and drain bias applied [4]. If $t_{31}$is changing to $t_{32}$ for a fixed $V_{31}$ (figure 2), the interface traps above $E_{F1}$ with a time constant $\tau_e$ verifying $t_{31}\tau_e< t_{32}$ will participate to the emission process. As $t_3$ becomes higher than the greatest time

constant of the traps, the emission process stops and these traps return in thermodynamic equilibrium with the energy bands. A saturation rate is reached for $t_3 = t_{sat}$. For values of $t_3$ above $t_{sat}$, the charge pumped during a cycle, when the transistor is switched to accumulation, remains constant and equal to the charge trapped in all interface states below $E_F$ ($E_F$ is determined by $V_3$). According to the Schockly-Hall-Read model (SHR theory) [5]. The time constant of a trap occupied by an electron is an exponential function of its energetic position $E_t$ in the silicon bandgap:

$$\tau_e = \frac{1}{v_{th}\sigma_n n_i \exp(-\frac{E_t - E_i}{KT})} \qquad (2)$$

Where $V_{th}$ is thermal velocity of electrons in silicon, $n_i$ the intrinsic carrier concentration and $E_i$ the intrinsic energy level. Then, it is possible to determine the energitic distribution of emission times and capture crosssection of electron traps by monitoring the charge pumped per cycle as a function of $t_3$ and $V_3$. The characteristic $Q_{it}$ $f(t_3)$ ($V_3$ fixed) saturates for a value of $t_3$ equal to $t_{sat}$ corresponding to the emission time constant of traps having an enrgy $E_t$ equal to the enregy of Fermi level. The value of the corresponding captur cross section can be written as:

$$\sigma_n = \frac{1}{v_{th_n} n_i t_{sat}} \exp(-\frac{E_t - E_i}{KT}) \qquad (3)$$

By selecting a duration of the third gate voltage level long enough that the quasi-totality of interface traps are indeed emitting their electrical charge, it is possible to calculate the energetic distribution of interface states density using the relation (1) and considering the variation of the charge pumped per cycle in saturationσn rate, as a function of $t_3$ and for different values of $V_3$.

## RESULTS AND DISCUSSION

The test devices were 0.5 μm MOS transistor. They presented an interdigital structure: the source and the drain form a single comb-shaped junction with the substrate that interpenetrates the "gate comb". Consequently, these devices require a very reduced area on the silicon wafer in spite of their great gate area (about 3200 $\mu m^2$) [6]. We have especialy tested these submicronic transistors at the beginning of the elaboration process, which explains the relatively high values of simullated interface states densities. Nevetheless, the sensitivity of our technique ($10^9$ states $eV^{-1}$ $cm^{-2}$) allows simulation of these devices during the entire process and after the differnet passivation annealings. The knowledge of the relation between the gate bias $V_g$ and the surface potential $\psi_s$ is required, in order to calculate the energetic distribution of emission times, capture cross sections and interface states density [7]. By using a frequency of 100 Hz, the resulting charge pumping current is low because $I_{cp}$ is proportional to $f(I_{cp}=f(Q_{it}))$. A low sensitivity results. In order to improve the sensittivity of the technique, we have directly simulated the current $I_{cp}$. For each duration of the third level, we can shoose the highest possible frequency that still maintains a quasi-equilibrium during accumulation and inversion times. Practicaly, frequency is not adjusted for each measurement but only threetimes for $t_3$ varying between 200 ns and 30 ms. A 10 KHz frequency is shosen $t_3<20$ ms, then for $20<t_3<800$ ms frequency is fixed to 1 KHz. And for $t_3$ >800 ms, frequency is reduced to 100 Hz. Times $t_{inv}$ and $t_{acc}$ are adjusted to be compatible with the gate voltage pulse period. The characteristic Icp vs log ($t_3$), shown on figure.3, is recorded for different values of the third-level voltage $V_3$. From the previous network of cuves for each voltage V3, the value of $t_{sat}$ corresponding to the beginning of the saturation of the pumped charge ($Q_{sat}$) can be easily determined.

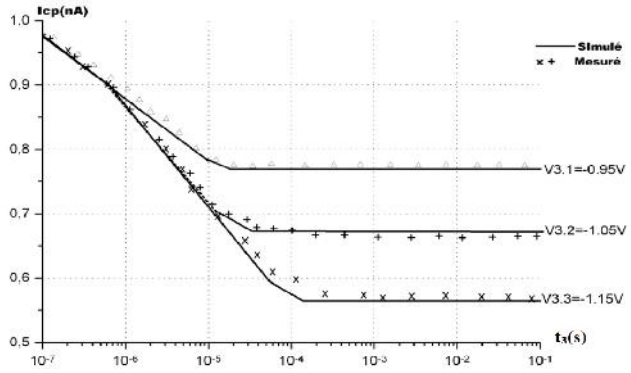


Figure.3 Pumped current in function of the intermediary tension level ($V_3$).

But the saturation times have not been determined like Saks and Ancona [2]. These authors define $t_{sat}$ as the abscissa of the intersection of the linear part of the $I_{cp}$ vs log($t_3$ ) saturation level characteristic with linear part of this curve for short $t_3$. Then the mean interface state density between $E_i$ and $E_{i+1}$ is given by:

$$D_{it}(E_m) = \frac{\Delta Q}{qA_{eff}\Delta E} = \frac{|Q_{i+1} - Q_i|}{|E_{i+1} - E_i|} \tag{4}$$

$$\text{With:} \quad E_m = E_i + \frac{E_{i+1} - E_i}{2} \tag{5}$$

The network of Icp (log ($t_e$), $V_3$) curves, shown figure 3, has been obtained on a n-channel transistor. Figure 4 shows the variation of pumped current a function of steep voltage.

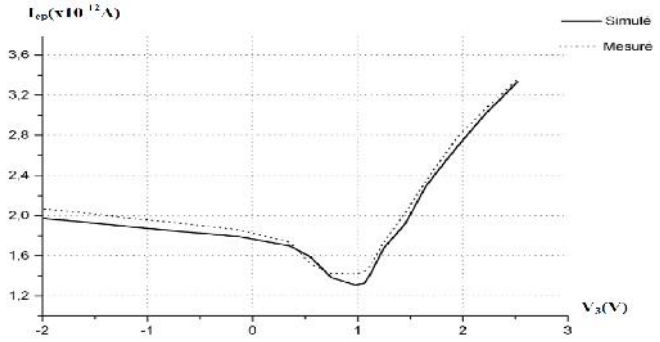

Figure.4 Densities current in function of the time transition intermediary tension level ($V_3$).

## CONCLUSION

We have set up, for the time a three-level charge pumping technique on industrial submicronic transistor. Although the nature of defects depends on the technological process. The validation of our model has provide results about pumping current in function the surface potential variation, the time (t) of pulse applied on the gate of MOS transistor, thus the characteristic of interface states in function of potential. In our work, we have developed a three level charge-pumping model implemented in Spice3F4. This model can be used to study the degradation of devices. All simulation results are compared with measured, the good accord has observed.

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